WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate having a main surface;

a pair of p-type impurity diffused regions formed at the main surface of said semiconductor substrate to serve as source/drain;

a floating gate formed on a region of said semiconductor substrate lying between the paired p-type impurity diffused regions with a tunnel insulating layer interposed between said floating gate and said semiconductor substrate; and

an impurity diffused control region formed at the main surface of said semiconductor substrate to control a potential of said floating gate.

2. The nonvolatile semiconductor memory device according to claim 1, wherein said impurity diffused control region is of p-conductivity type and faces said floating gate with an insulating layer interposed therebetween.

3. The nonvolatile semiconductor memory device according to claim 1, wherein said impurity diffused control region is a pair of source/drain impurity diffused regions formed at the main surface of said semiconductor substrate such that a region of said semiconductor substrate positioned below said floating gate is interposed between the paired source/drain impurity diffused regions.

4. The nonvolatile semiconductor memory device according to claim 3, wherein said pair of source/drain impurity diffused regions is of n-conductivity type.

5. The nonvolatile semiconductor memory device according to claim 4 further comprising a p-type well region formed at the main surface of said semiconductor substrate, wherein said pair of n-conductivity type source/drain impurity diffused regions is formed in said p-type well region.

6. The nonvolatile semiconductor memory device according to claim 3, wherein said pair of source/drain impurity diffused regions is of p-conductivity type.

7. The nonvolatile semiconductor memory device according to claim 6 further comprising an n-type well region formed at the main surface of said semiconductor substrate, wherein said p-conductivity type source/drain impurity diffused region is formed in said n-type well region.

8. The nonvolatile semiconductor memory device according to claim 1, wherein said impurity diffused control region is of n-conductivity type and faces said floating gate with an insulating layer interposed therebetween.

9. The nonvolatile semiconductor memory device according to claim 8 further comprising a p-type well region formed at the main surface of said semiconductor substrate, wherein said impurity diffused control region of n-type is formed in said p-type well region.

10. The nonvolatile semiconductor memory device according to claim 1 further comprising:

a field insulating layer formed at the main surface of said semiconductor substrate between a region where said pair of p-type impurity diffused region is formed and a region where said impurity diffused control region is formed; and

a p-type impurity diffused region for device isolation formed at said semiconductor substrate just below said field insulating layer.